oxidation growth process is carried out to consume the underlying epitaxial silicon. This option avoids the need for a uniform silicon etch rate across the wafer as well as from wafer to wafer.

[0030] Once the epitaxial silicon is thinned in the region for the fully depleted CMOS, the method continues as shown in FIG. **4**. Here, the pad nitride is stripped off (e.g., using a hot phosphoric dip). Similarly, all oxide can be removed (e.g., using a hydrofluoric acid). As can be seen, the resulting structure includes a thinned region of silicon for fully depleted CMOS, and a thicker region of silicon for photonics and/or partially depleted CMOS.

[0031] The method continues as shown in FIG. **5**, wherein a new two-layer hardmask is deposited as explained before using pad oxidation (for lower oxide layer) and pad nitride deposition (for upper nitride layer). The thicknesses for each of the oxide and nitride layers as well as the specific materials themselves can be, for example, the same as the previous hardmask. The initial pattern for the waveguides and any active areas for thick CMOS region is then applied to the two-layer hardmask, where photoresist (resist) is applied to areas that are to be preserved. As is known, an "active area" is a semiconductor term which defines the areas where electronic components (e.g., MOSFETs or other such gate-level components and modulators, salicide structures, etc) will be located. This standard electronics layer is combined into the photonics layer, and both layers are processed as one in an efficient manner that avoids etching non-uniformities associated with conventional techniques. Note that in other embodiments, two masks could be used to define the electronics (e.g., CMOS) and photonics (e.g., channel and ridge waveguides) separately. Further note that a resist mask could be used over the step region if so desired, but this may likely cause subsequent particle issues. Other such variations will be apparent in light of this disclosure.

[0032] The method continues as shown in FIG. **6**, wherein an initial etch is performed on the patterned hardmask to remove unmasked pad nitride and pad oxide layers, as well as portions of the epitaxial silicon layer. The amount removed of the epitaxial silicon layer depends on the region being etched. In more detail, this initial etch is a partial etch of the silicon region for photonics and thick CMOS, and leaves a prescribed amount of silicon on top of the buried oxide, so that the remaining epitaxial silicon can be used for the slab region of forthcoming modulators. As can be seen, the hardmask remains on top of the waveguide structures (which in this example embodiment happen to include a channel waveguide, and a ridge waveguide included in the ring modulator), and acts as an etch mask again during subsequent etching steps (e.g., waveguide slab mask etch). In contrast, this initial etch is a full etch of the thinner silicon region for fully depleted CMOS, where the etch of that region reaches the buried oxide layer. At point A shown in FIG. **6**, note that there may be silicon undercut due to relatively long overetch. In addition, at point B, note that there may be an nitride/oxide rail at the transition point (step region), depending on etch selectivity. Once this initial etch of both the thin region (full etch) and thick region (partial etch) is completed, the resist is then stripped.

[0033] The method continues as shown in FIG. **7**, where the region for photonics (or thick CMOS) is patterned to have slabs (for the ring modulator), and body contacts (for partially depleted CMOS). The resist is deposited as shown. Note that point C can also be protected with resist, or point C can be left exposed for more nitride/oxide/silicon etching if necessary. The method continues as shown in FIG. **8**, where the second part of the initial etch (discussed with reference to FIG. **6**) is performed to completely pattern the epitaxial silicon in the region for photonic and thick CMOS. The resist is then stripped. Note the resulting slab portions of the ring modulator. Again, at point B there may be an nitride/oxide rail at the transition point (step region), depending on etch selectivity. Standard photolithography (including suitable resist materials) can be used for the slab patterning and etching depicted in FIGS. **7** and **8**.

[0034] The method continues as shown in FIG. **9**, where a wafer clean (e.g., Huang clean) is performed. Alternatively, this clean step may be replaced with a resist mask and hydrofluoric acid dip to undercut the pad oxide in CMOS regions. Undercutting the pad oxide leads to increased rounding (larger radius curve) at the top corners of active areas, which can be seen after subsequent oxidations. Typically for CMOS, the increased rounding is desired. A resist mask may be used to block the hydrofluoric acid exposure to photonic devices, if desired. Then, liner oxidation is carried out so that the remaining epitaxial silicon is provided with an oxide layer as shown. Liner oxidation minimizes dry etch damage on the top and sides of CMOS active areas and the sides of the waveguides. The liner oxide can be, for example, the same as the pad oxide and/or buried oxide. In addition, any desired slab implants (e.g. for ring modulator) can be completed using a photolithography (e.g., resist and etch), implant, and resist strip sequence. Again, at point B, there may be a nitride/oxide rail at the transition point (step region proximate the isolation region), depending on etch selectivity.

[0035] The method continues as shown in FIG. **10**, where an oxide fill process is performed (i.e., the shallow trench isolation regions are filled). The oxide used for the fill can be, for example, the same as the pad oxide and/or buried oxide. In one particular embodiment, an HDP-CVD oxide is used for the oxide fill process. The patterning of the oxide thinning mask can be carried out, for example, as previously discussed with reference to FIG. **1**, using standard photolithography techniques, thereby protecting (with resist) the region for photonics/thick CMOS and exposing the region designated fully depleted CMOS (or other circuitry/structure that requires a thinned region). Note that the dimensions of the oxide thinning mask (i.e., resist) can be varied to modify the transition region as desired. At point D, note that the transition region can be left exposed or protected with resist, depending on desired attributes of transition region.

[0036] As can be seen with reference to FIG. **11**, the method continues with an oxide etch (e.g., dry etch) to remove the bulk of oxide above the fully depleted CMOS active region and any unprotected isolation region. This etch process can be used to reduce polish load on the CMOS side. The method continues with stripping the resist. In other embodiments, note that the oxide etch could be eliminated by substituting a selective CMP process. In such case, a CMP dish-out process may be used to thin the oxide in the fully depleted CMOS regions. Whether etching or polishing is used depends on factors such as desired polish load or etch load, CMP and/or dish-out capability, desired processing time, etc.

[0037] As can be seen with reference to FIG. **12**, the method continues with a chemical mechanical polish (CMP) process, so as to polish all oxide down to the underlying pad nitride. Note the dish-out technique discussed in the previous section actually polishes down to the pad nitride, so the methodology